Sensitivity of Planar Slot Array Antennas to Manufacturing Tolerances

Ahmad Bakhtafrouz and Amir Borji*
Department of E&CE, Isfahan University of Technology, Isfahan 84156, Iran
E-mail: aborji@cc.iut.ac.ir

INTRODUCTION

Waveguide slot arrays are an attractive but expensive choice in a wide range of microwave and millimeter-wave applications when high gain and efficiency are critical. Resonant longitudinal slot arrays offer very high aperture efficiency, low side-lobe levels, and low cross polarization, however, they usually suffer from narrow bandwidth and high cost due to high precision required in manufacturing.

When designing the array, slot offsets and lengths are calculated by an iterative algorithm which minimizes the input return loss [1]. The manufacturing process always introduces some errors depending on the accuracy of milling machines or etching process, so the offsets and lengths of radiating slots will be different from design values. These differences can have a major impact on the impedance matching of antenna and degrade its return loss substantially. Moreover, noticeable degradation may occur in side-lobe levels.

Recently, frequency analysis of waveguide slot arrays has been studied by many authors [2,3]. They focus on the analysis of array performance at frequencies different from the array design frequency. Such analysis procedure is proved to be very useful for evaluating the sensitivity of antenna parameters to mechanical tolerances.

In this paper, the effect of manufacturing errors on the return loss and radiation pattern of planar slot arrays is studied for the first time. For this purpose a 16 element square array that is presented by the authors in [4] is considered and the algorithm of array analysis described in [3] is implemented in MATLAB.

ANALYSIS PROCEDURE

For a specific planar array of M slots, the slot offsets x_{tn} and slot lengths $2l_{tn}$ are given. The first and second basic design equations given by Elliott [1] still apply at frequencies other than the design frequency. Combining these equations yields:

$$K_2 \frac{f_{tn}^2}{y_n^{self}} V_{tn}^s + \sum_{j=1,\ j\neq i}^{M} V_j^s g_{ji} + \frac{K_2}{K_3}\left[V_{t,n-1}^s\ h_{tn}\ h_{t,n-1} + V_{t,n+1}^s\ h_{tn}\ h_{t,n+1}\right] = \frac{K_2}{K_1} f_{tn}\ V_{tn} \tag{1}$$

978-1-4244-3647-7/09/$25.00 ©2009 IEEE

The constants K_1, K_2 and K_3 and functions g_{ji}, f_{tn}, h_{tn} and y_n^{self} are given in [3]. Above formula can also be written in a matrix form [3]. V_{tn} is the mode voltage at the tn^{th} slot of array which is calculated based on the algorithm given in [3]. The unknown slot voltages, V_{tn}^s, can then be obtained by solving the above system of linear equations. After finding the slot voltages, one can compute the active admittance of each radiating slot using the following expression [3]:

$$y_{tn}^a = 1 \Bigg/ \left\{ \frac{1}{y_{tn}^{self}} + \frac{1}{f_{tn}^2 K_2} \sum_{j=1,\ j\neq i}^{M} \frac{V_j^s}{V_i^s} g_{ji} + \frac{1}{f_{tn}^2 K_3} \left[\frac{V_{t,n-1}^s}{V_{tn}^s} h_{tn} h_{t,n-1} + \frac{V_{t,n+1}^s}{V_{tn}^s} h_{tn} h_{t,n+1} \right] \right\} \tag{2}$$

Now, using the above active admittances, new values of V_{tn} and, subsequently, new values of slot voltages can be obtained from (1). This process must be repeated until the values of V_{tn}^s converge. Six to eight iterations are usually sufficient to ensure convergence. At the end of analysis procedure return loss of the entire array is calculated from the transmission-line model of the array and final values of y_{tn}^a [3]. Moreover, gain and side-lobe levels of antenna may be obtained from equation (32) of [3] with final values of slot voltages, V_{tn}^s.

NUMERICAL RESULTS

Here, we considered the 4×4 element slot array presented in [4] for sensitivity analysis. This array was designed and manufactured at 60GHz and is completely based on substrate integrated waveguide (SIW) technology. The array consists of two PCB layers: on the top layer radiating slots are etched on the broad wall of four side by side SIWs and on the bottom layer a single SIW feeds these four branches. Couplings between the two layers are achieved through slanted slots [4]. Note that, in this analysis, the waveguides have solid walls and they are equivalent to substrate integrated waveguides in the actual array. Furthermore, it is assumed that the maximum error in etching process is about 15μm.

Fig.1 shows the return loss for three different cases: in (a) the return loss obtained for the nominal design is given and it is seen that both HFSS and our analysis program produce very similar results, in (b) slot offsets remain unchanged but the lengths of all radiating slots are reduced by 30μm, and in (3) again the slot offsets are those of the nominal design but all slot lengths are enlarged by 30μm. Fig.2 shows S_{11} for the above cases with the exception that all slot offsets are now reduced by 15μm from their nominal values. Finally, Fig.3 shows S_{11} of the same antennas except that the slot offsets are now 15μm larger than original values obtained from the design algorithm. Fig.1-3 show that how the center frequency

of array depends on slot lengths and offsets. A 30μm change in slot lengths causes 500MHz deviation in operation frequency. It is also interesting to note that a 30μm deviation in slot lengths has almost the same impact as 15μm change in slot offsets. Fig. 4 compares the gain of the original array with that of the array in which all slot offsets and lengths have changed by 15μm and 30μm, respectively, which is the worst case scenario. It is clear that side lobe levels are not significantly affected.

CONCLUSION

Sensitivity of planar waveguide slot arrays to manufacturing tolerances was analyzed. Results of such analysis can be very useful for the antenna designer as well as the manufacturer when mass production is considered. Obviously in practice the errors are distributed randomly among the dimensional parameters and a thorough statistical analysis of the array performance is necessary. Such investigation is currently under way by the authors and the results will be presented in a separate paper.

REFERENCES

[1] R. S. Elliott, "An improved design procedure for small arrays of shunt slots," *IEEE Trans. Antennas Propagat.*, vol. 31, pp. 48–53, Jan. 1983.

[2] G. A. Casula and G. Mazzarella, "A direct computation of the frequency response of planar waveguide slot arrays," *IEEE Trans. Antennas Propagat.*, vol. 52, no. 7, pp. 1909-1912, July. 2004.

[3] J. C. Coetzee, J. Joubert and D. A. McNanamara, "Off-center-frequency analysis of a complete planar slotted-waveguide array consisting of sub-arrays," *IEEE Trans. Antennas Propagat.*, vol. 48, no. 11, pp. 1746-1755, Nov. 2000.

[4] A. Bakhtafrouz and A. Borji, "Compact two-layer slot array antenna with SIW for 60GHz wireless applications," submitted to 2009 IEEE AP-S Symposium

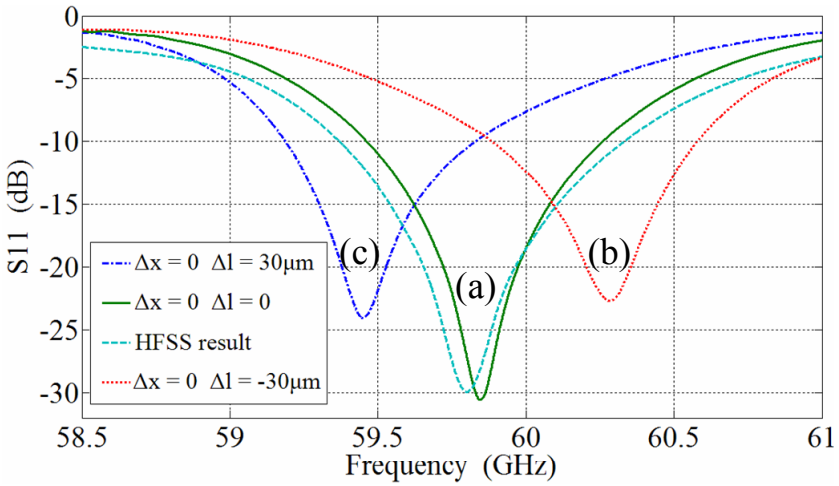

Fig.1: S11 for three cases where slot offsets remained equal to original design values

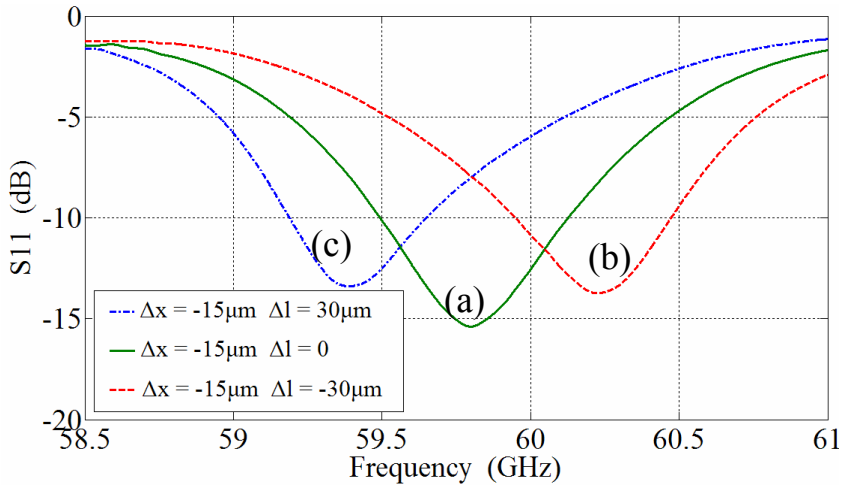

Fig.2: S11 for three different slot lengths. Slot offsets reduced from their nominal values

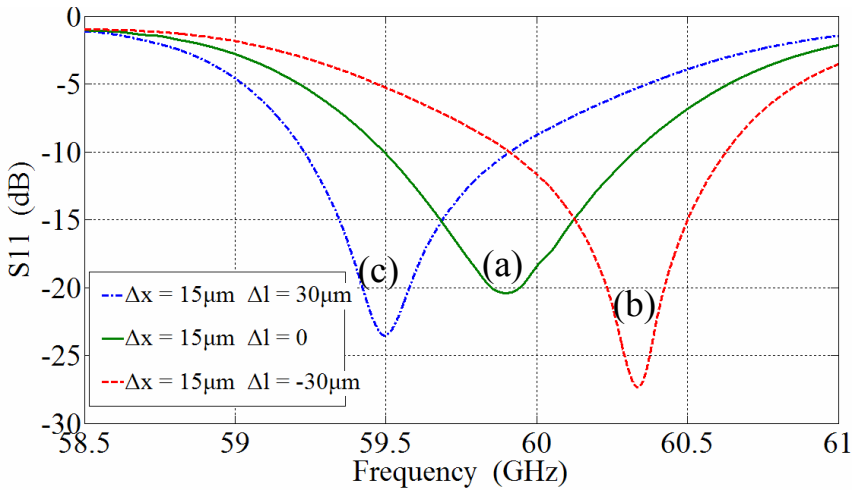

Fig.3: S11 for three different slot lengths. Slot offsets increased from their nominal value

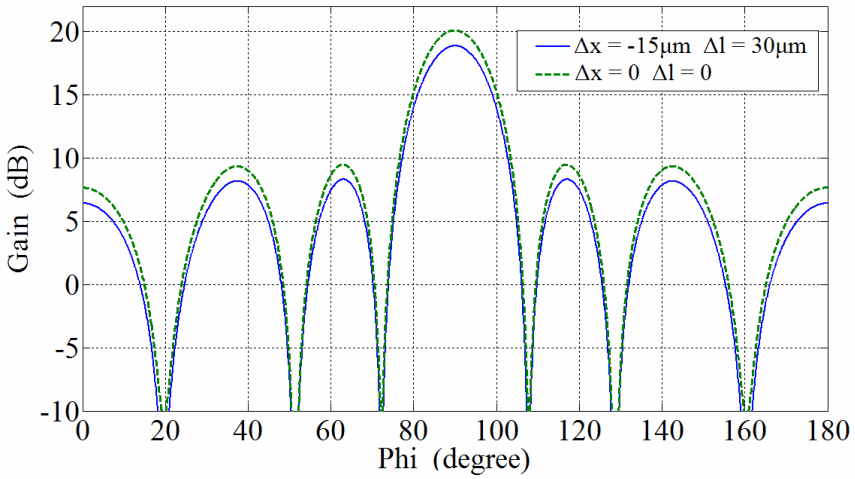

Fig.4: Gain of the original array and that of the worst case array at 60GHz