On-Chip Communications

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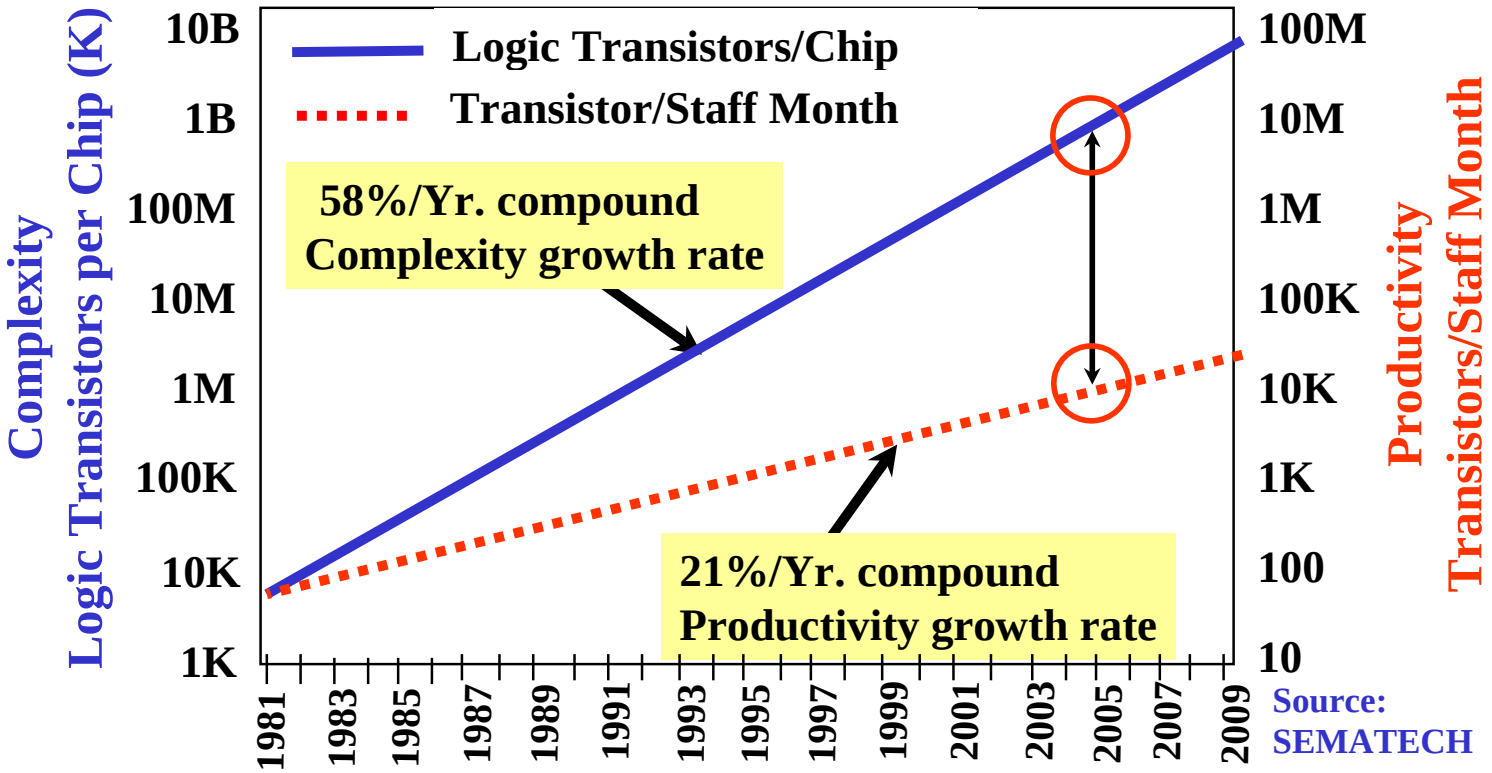
Introduction

Adapted with modifications from lecture notes prepared by S.Pasricha and N.Dutt

Outline

- Introduction to SoC Design Trends
- Significance of on-chip communication architectures

Designer Productivity Gap

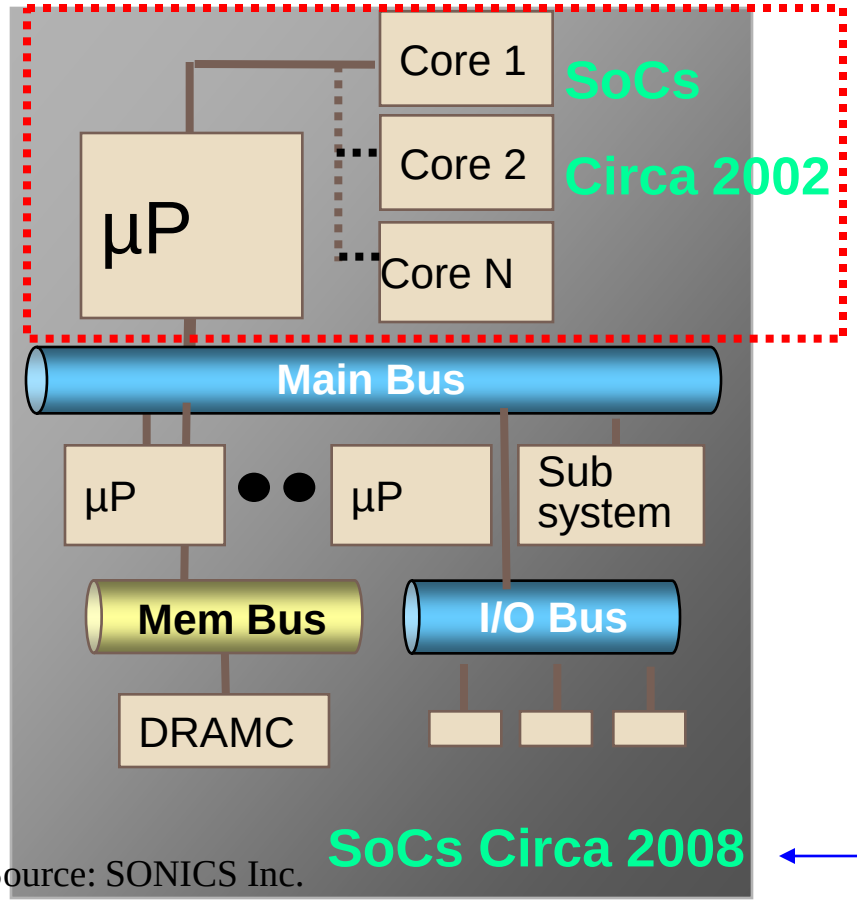


SoC designs today are complex, characterized by more and more IPs being integrated on a single chip, and a shrinking time-to-market

Coping with SoC Complexity

- Practicing IP based Design and Reuse
  - Raising the reuse factor from standard cells to IP blocks
    - e.g. predesigned hardware IPs for processors (ARM, PowerPC), communication (AMBA, CoreConnect), memories (Samsung SDRAMs, Denali SRAMs), I/O (UART, USB) etc.
  - IPs not just for hardware, but for software (device drivers, OS) too
  - Substantial reduction in SoC design and verification time
  - Requires initial investment to create reusable cores
    - but productivity improves with reuse
- IP Interfacing Standards
  - IP based design needs to handle incompatible IP interfaces
  - Assembling heterogeneous IPs for SoC design can take months!!!
  - Need for unified standard to quickly connect IPs
    - e.g. OCP-IP, VSIA VCI etc.

Major SoC Design Challenge



Source: SONICS Inc.

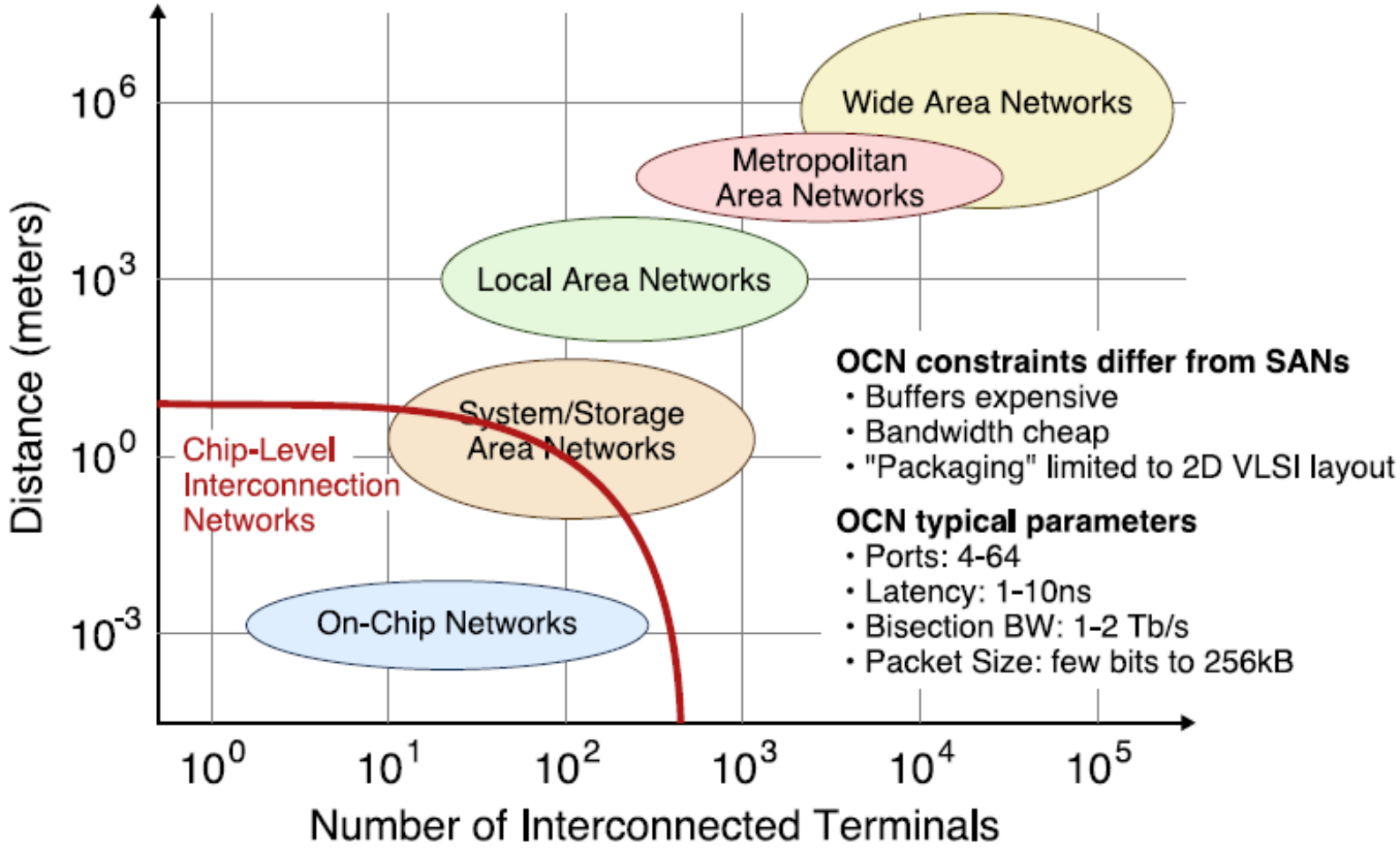
Critical Decision Was uP Choice

- Exploding core counts requiring more advanced Interconnects
- EDA cannot solve this architectural problem easily
- Complexity too high to hand craft (and verify!)
- Data flow replacing data processing as major SoC design challenge

Critical Decision Is Interconnect Choice

Communication Architecture Design and Verification becoming Highest Priority in Contemporary SoC Design!

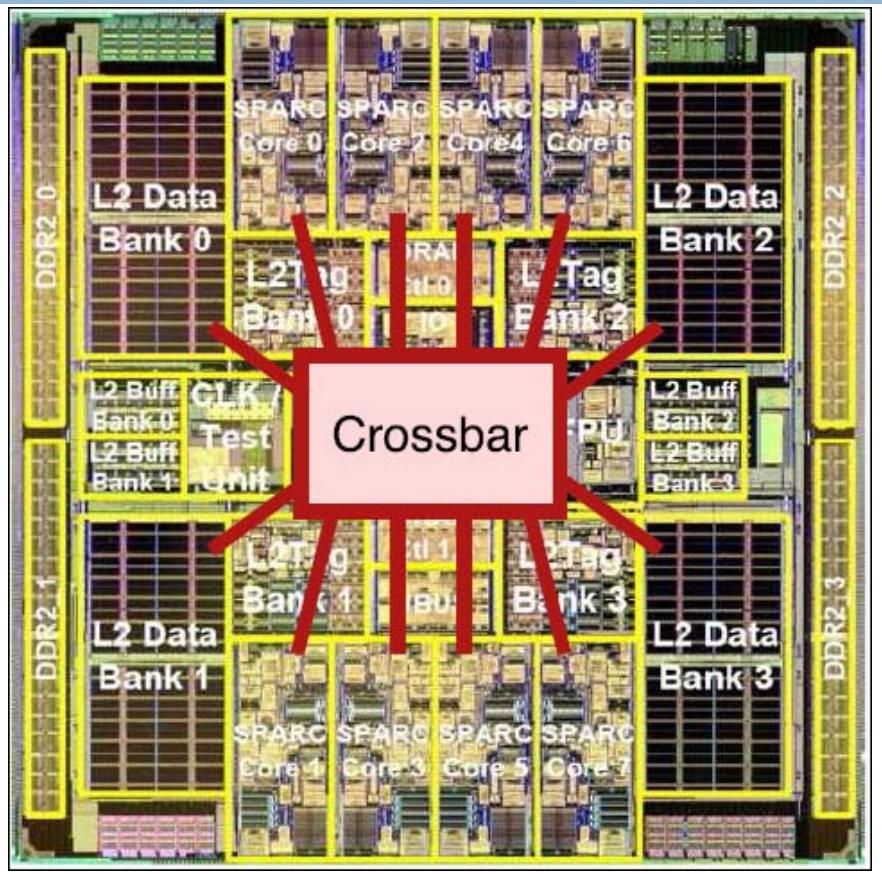
Types of Interconnection Networks



Examples of On-chip Communication Architectures:

Sun Niagara Processor

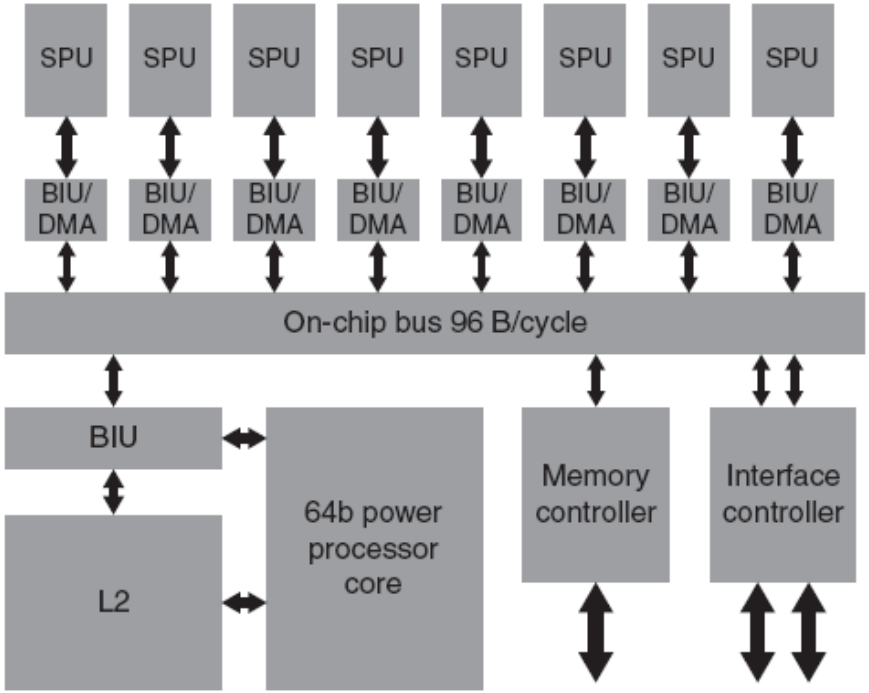
- 8 multithreaded processors
- Single-stage crossbar connecting 8 cores to 4 L2 cache banks
- 200 GB/s total bisection BW

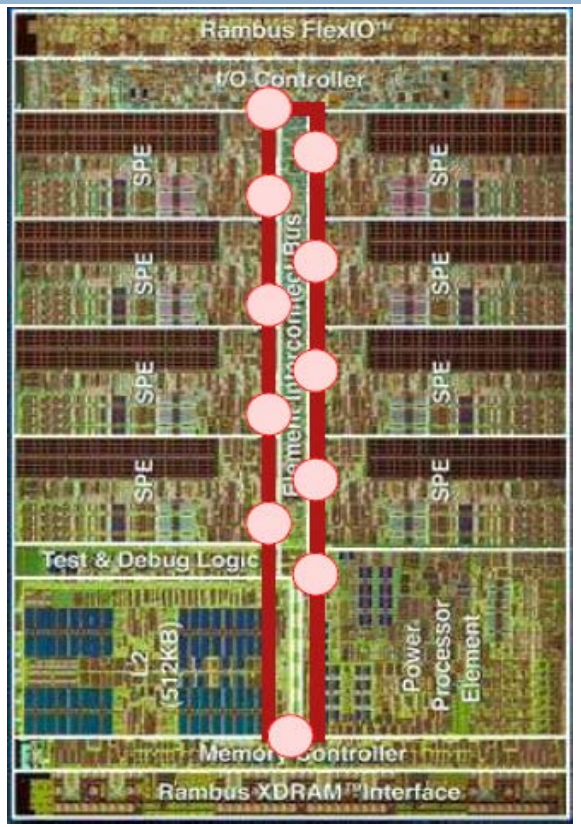


Examples of On-chip Communication Architectures:

IBM Cell Processor

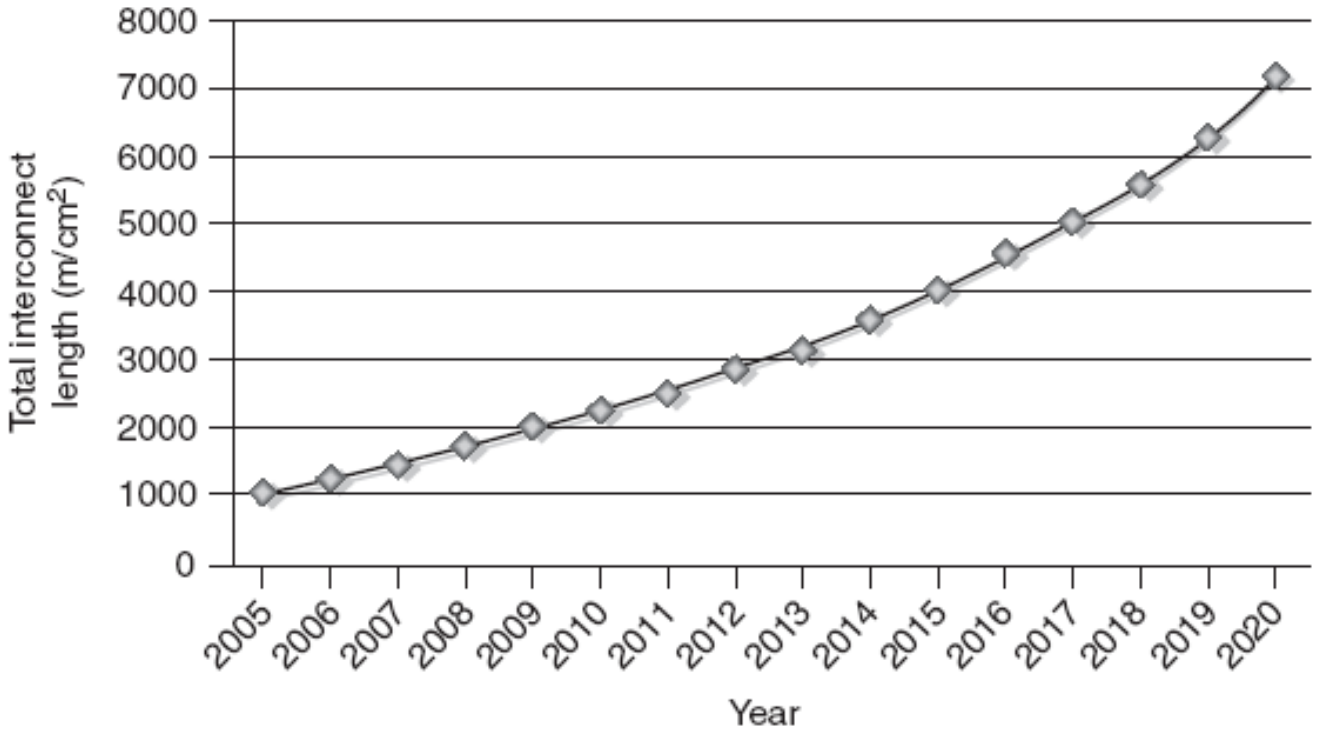
- 1 general-purpose processor
- 8 processors specialized for data-parallelism
- 4 uni-directional rings, each is 128b wide at 1.6 GHz
- Network Bisection BW = 25.6 GB/s
- Total Bisection 102.4 GB/s





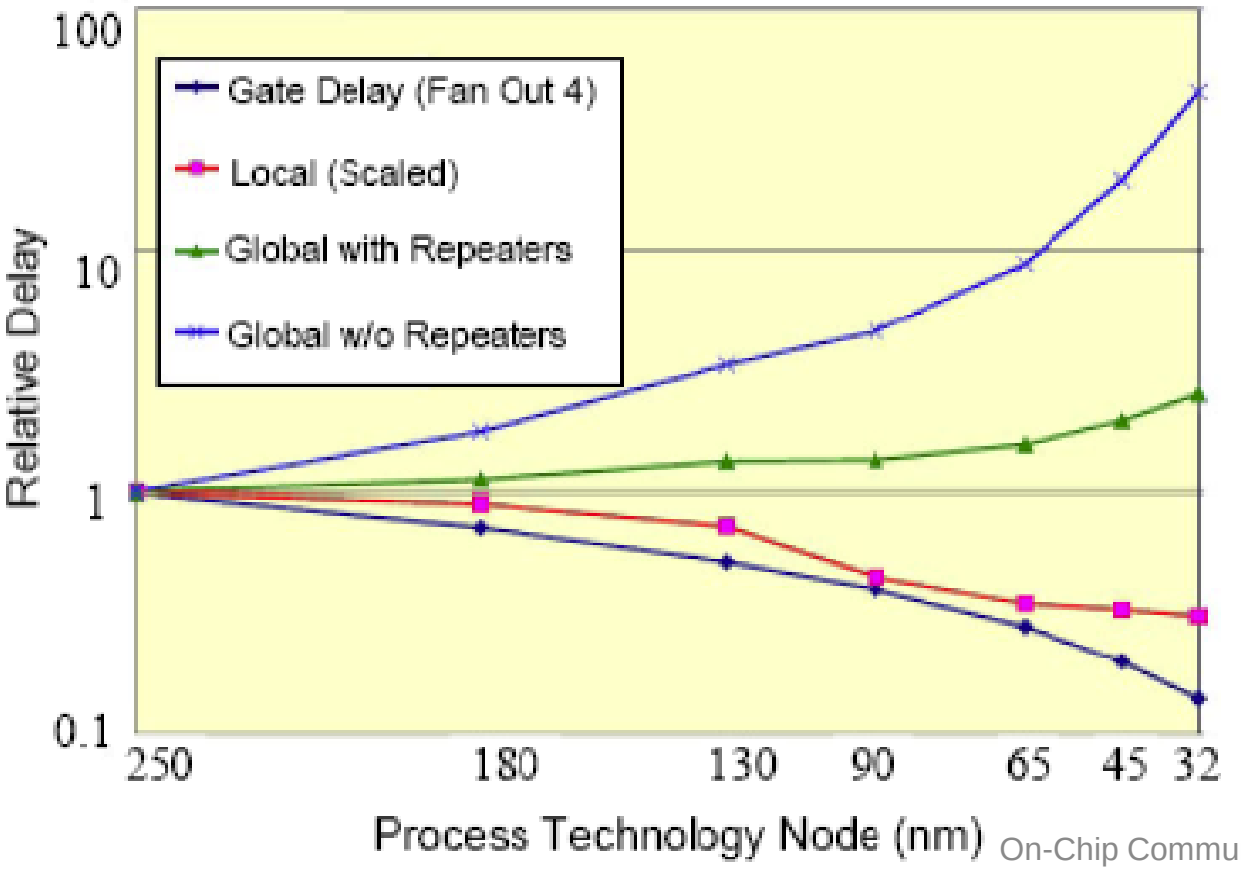
Technology Scaling Trends: Total Interconnect Length on a Chip

- Highlights importance of interconnect design in future technologies



Technology Scaling Trends: Interconnect Performance

- Relative delay comparison of wires vs. process technology
- Increasing wire delay limits achievable performance

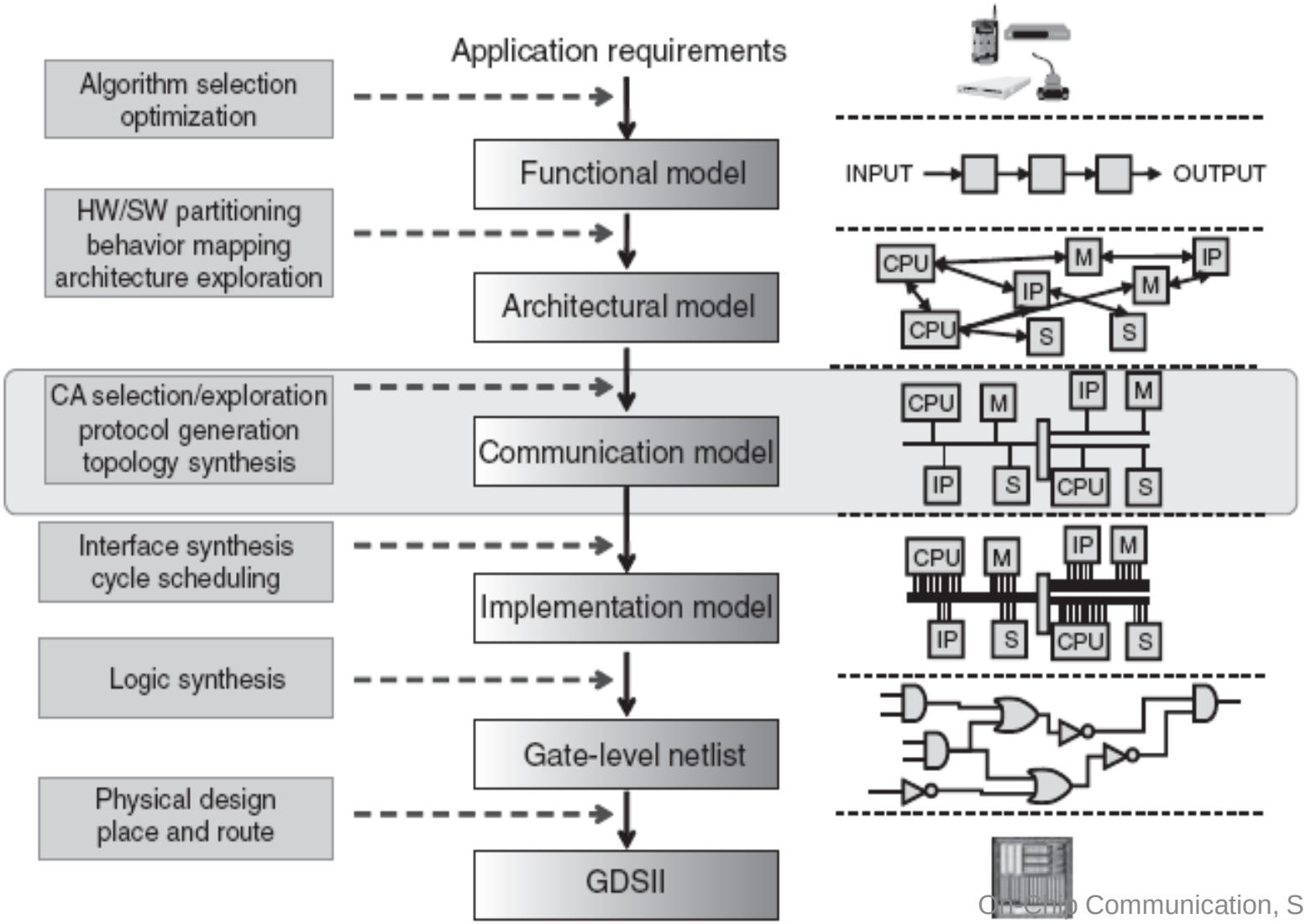


Need for Communication-Centric Design Flow

- Communication is THE most critical aspect affecting system performance
- Communication architecture consumes up to 50% of total on-chip power
- Ever increasing number of wires, repeaters, bus components (arbiters, bridges, decoders etc.) increases system cost
- Communication architecture design, customization, exploration, verification and implementation takes up the largest chunk of a design cycle

Communication Architectures in today's complex systems **significantly** affect performance, power, cost and time-to-market!

Ideal ESL Design Flow



Course Syllabus

- **CHAPTER 1 Introduction**
- **CHAPTER 2 Basic Concepts of Bus-Based Communication Architectures**
  - Topology types
  - Physical structure
  - Clocking
  - Arbitration and decoding
  - Data transfer modes
  - Physical implementation issues
  - DSM effects
- **CHAPTER 3 Networks-On-Chip**
  - Network Topology
  - Switching Strategies
  - Routing Algorithms
  - Flow Control
  - Clocking Schemes
  - Quality of Service

Course Syllabus

- **CHAPTER 4 Test and Fault Tolerance for NoC Infrastructures**
  - Test Methods for NoC Fabrics
  - Fault Models for NoCs
  - Addressing Reliability of NoC Fabrics through Error Control Coding
  - Power-Reliability Trade-Off
- **CHAPTER 5 Energy and Power Issues in Network-on-Chips**
  - Models for Power Estimation of Wires
  - Models for Power Estimation of On-Chip Communication Architectures
  - Models for Thermal Estimation
  - Energy and Power Reduction Techniques in NoC
- **CHAPTER 6 Three-Dimensional on-Chip Communication Architectures**
  - Three-Dimensional Integration of Integrated Circuits
  - Physical Analysis of NoC Topologies for 3-D Integrated Systems
  - 3-D NoC on Inductive Wireless Interconnect

Course Syllabus

- **CHAPTER 7 Emerging On-Chip Interconnect Technologies**
  - Optical Interconnects
  - RF/Wireless Interconnects
  - CNT Interconnects
- **CHAPTER 8 Silicon-on-Insulator (SOI) Photonics**
  - Silicon-on-Insulator Waveguides
  - Refractive Index and Loss Coefficient in Optical Waveguides
  - Optical Modulation Mechanisms in Silicon
- **CHAPTER 9 Optical on-Chip Interconnects**
  - Silicon Photonics: Advantages and Drawbacks
  - Photonic opportunity for NoCs
  - Photonic Switches
  - Electrically-Assisted NoCs
  - All-Optical NoCs

Textbooks

- De Micheli, Giovanni, and Luca Benini. **Networks on chips: technology and tools**. Morgan Kaufmann, 2006.
- Pasricha, Sudeep, and Nikil Dutt. **On-chip communication architectures: system on chip interconnect**. Morgan Kaufmann, 2010.
- Gebali, Fayez, Haytham Elmiligi, and Mohamed Watheq El-Kharashi, **Networks-on-chips: Theory and Practice**. CRC Press, 2011.
- Jantsch, Axel, and Hannu Tenhunen**. Networks on Chip**. Springer, 2006.
- Pavesi, Lorenzo, and Gérard Guillot. **Optical Interconnects: The Silicon Approach**, *Springer, 2006*.
- Reed, Graham T., and Andrew P. Knights. **Silicon photonics: An Introduction**. Wiley, 2004.

Grading Structure

- Final Exam: 50%
- Midterm Exam: 30%
- Project: 20%